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Addressing Performance and Reliability Concerns with Thermal Analysis for RF Power Applications

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RF Summit, Espoo 2024

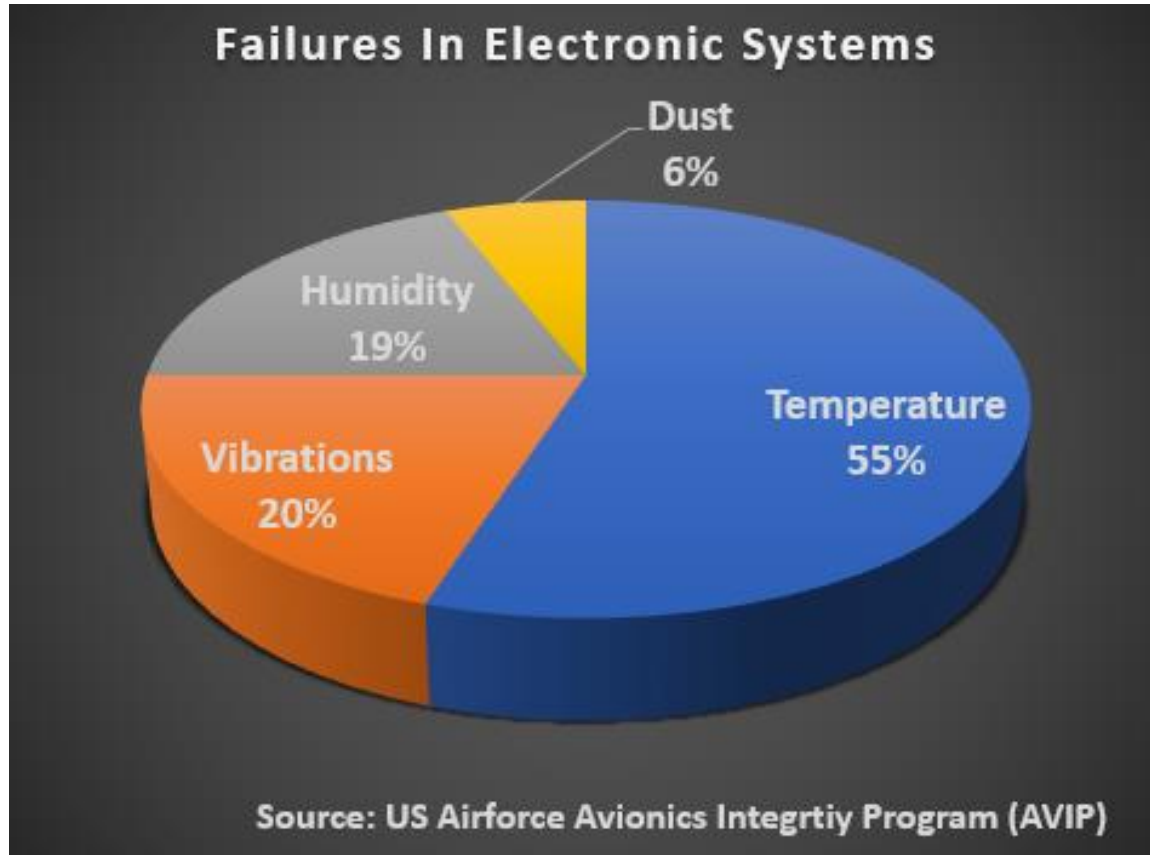
Overview

- Thermal Challenges
 - Reliability
 - Performance
 - Design flow bottlenecks
- In-Design Enablement
 - Thermal Analysis Options
 - Microwave Office In-Design Thermal Analysis
- Summary



Thermal Challenges

Thermal Design – A Key Concern for Electronics Design

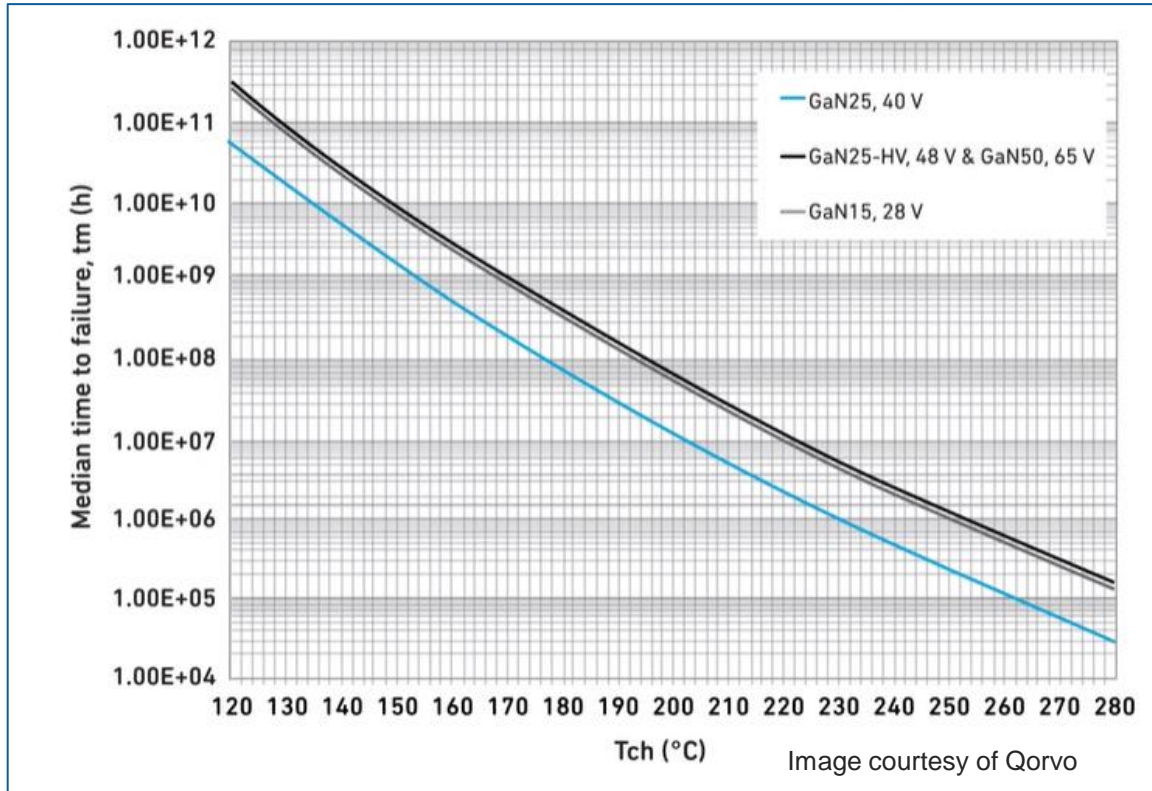


- Reliability / product life-time degradation
 - Increased component stress
 - Component parameter drift
 - Open / short circuits
 - Thermal run-away
 - ...
- Performance degradation
 - Nonlinearity
 - Efficiency
 - Increase in noise-sensitivity
 - Device temperature bias mismatch
 - Shortening burst duration
 - ...
- ...

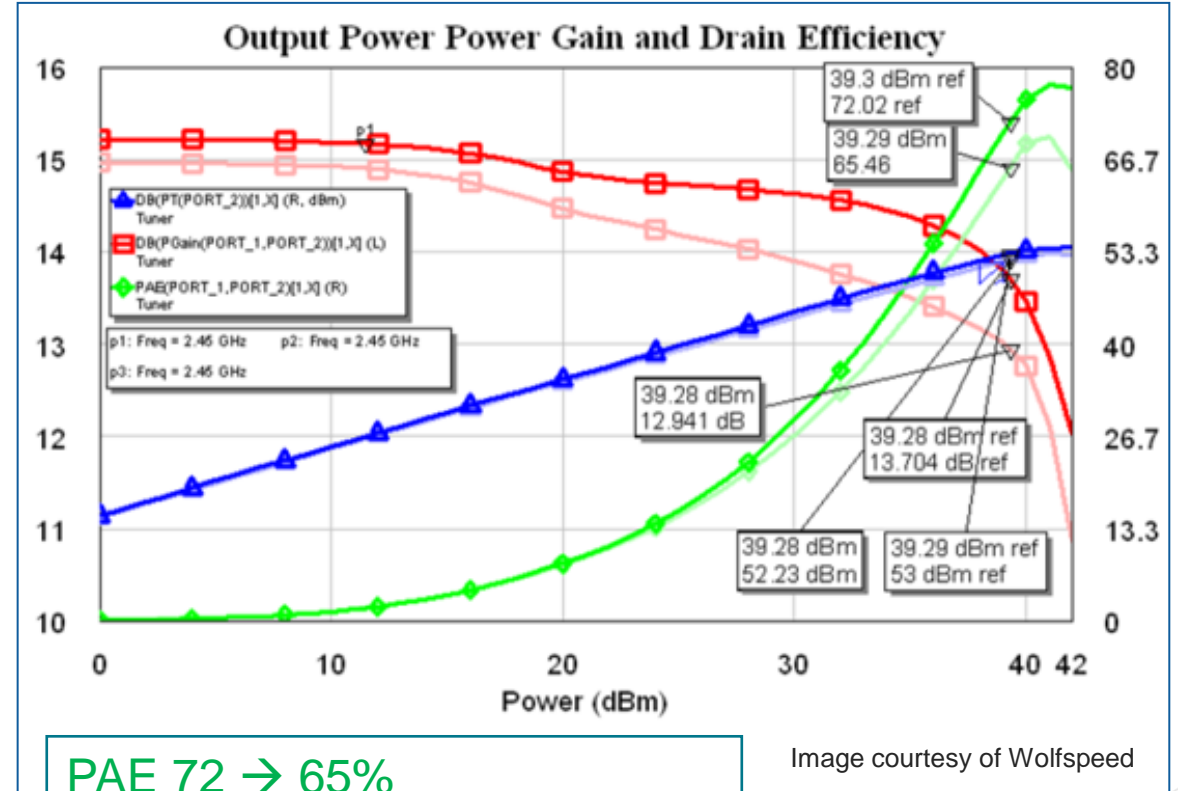
The Effects of Temperature On Electronics

GaN HEMT High Power Amplifiers

- Time to Failure vs Temp



- Performance w / wo self-heating

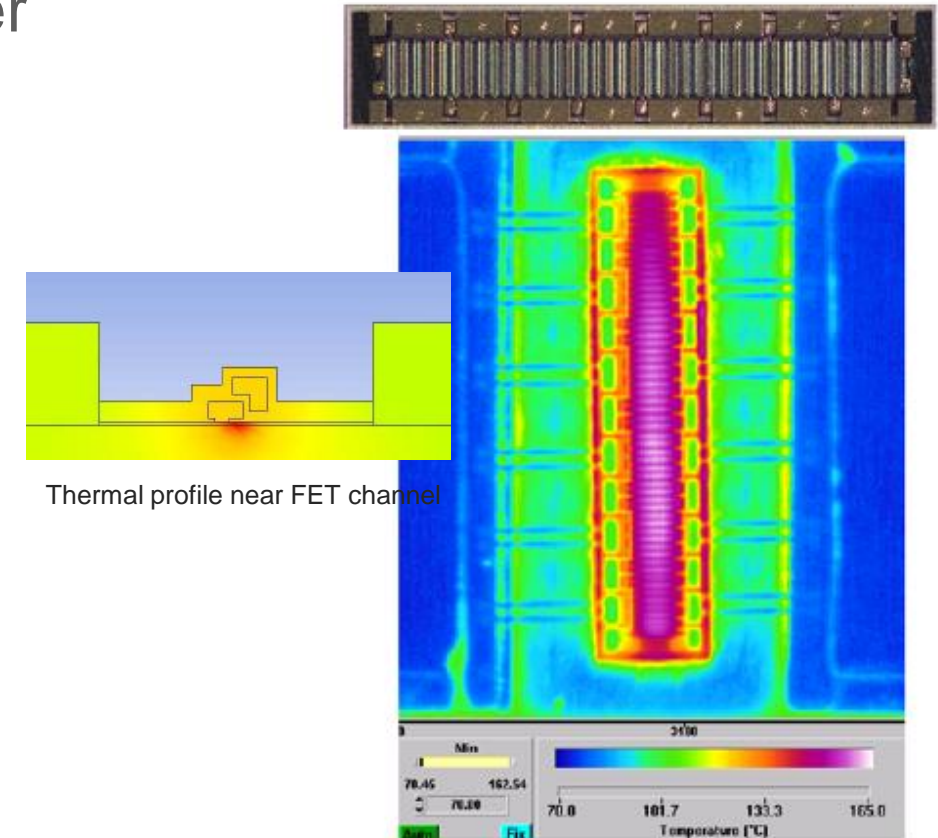


PAE 72 → 65%
Power Gain 13.7 → 12.9 dB

Heat Generation in PAs

Typical Heat development in a GaN Power Amplifier


- A GaN HEMT with gate periphery of 28.8mm operating at 28 volts drain voltage delivers 120 Watts CW
- For 60% DC to RF conversion efficiency there will be 80 Watts dissipated heat
- For an active chip area of 2.5 mm², the gate heat density exceeds 32 watts per mm² / 3.2kW per cm²
- This heat must be dissipated from the device channel through the heatsink and the package / and PCB so requires **detailed** analysis of the **conduction path** including the FET layout – this is not suited for traditional Thermal CFD simulations



Infrared thermal measurement of 28.8mm GaN HEMT
Image courtesy of Cree

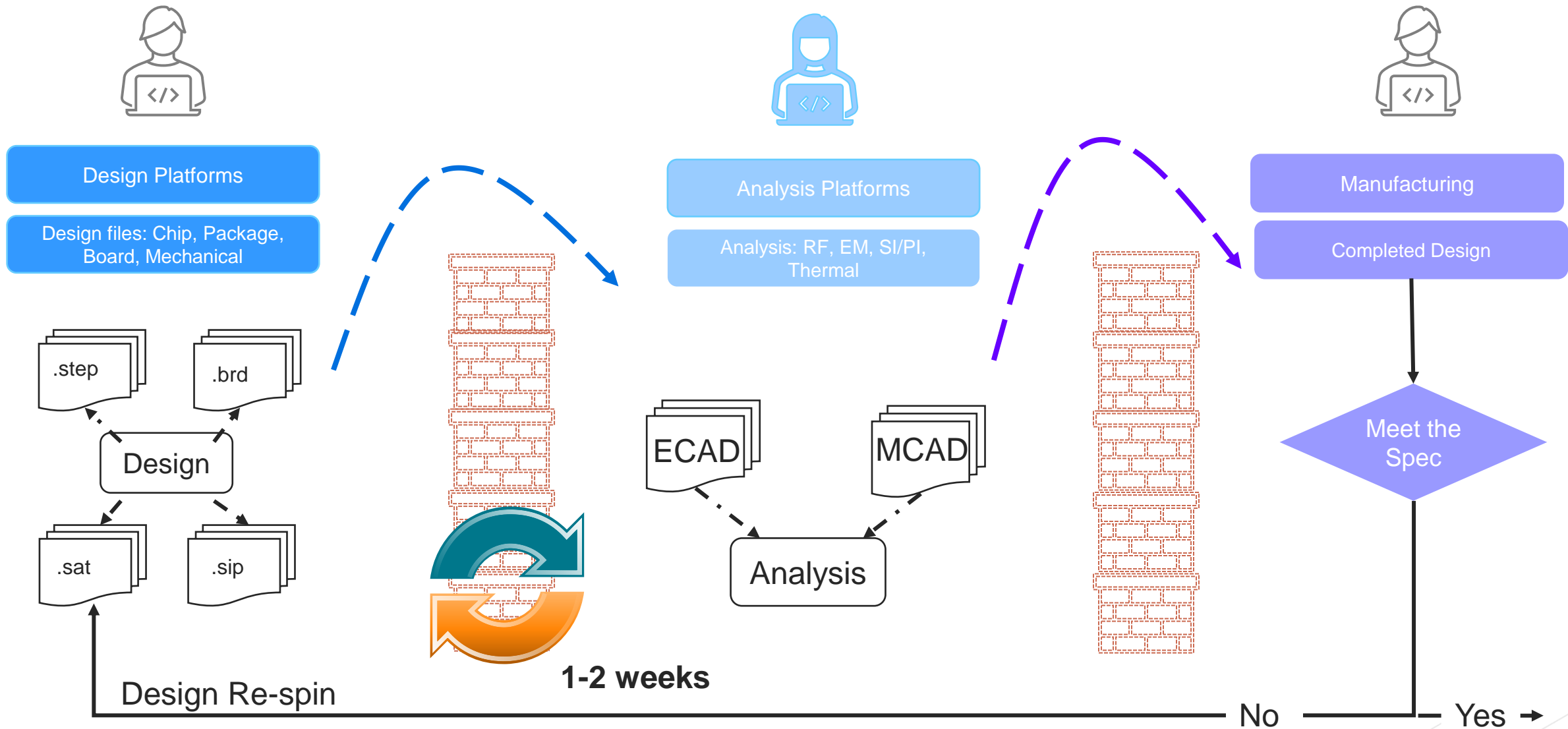
Status

- The Cost of Heating
 - Reliability degradation / failure
 - Performance degradation
- Heat mitigation is required
 - Lower operating power – reduces performance
 - Impacts mobile & radar range, data rates, etc.
 - Increase heatsinking
 - increases cost, size, weight, complexity
- Desired solution
 - Address excessive heat with minimal mitigation to reduce impact on performance, costs, etc.
 - Minimize impact on engineering turnaround time

A black clothespin is attached to a thin, dark string that stretches across the top of the frame. The clothespin is holding a small, white rectangular card. The card is centered horizontally and contains text. The background is a plain, light grey surface.

With these well known
challenges, why is
thermal analysis not
done more regularly
today in RF designs?

Multiple Platform and Lack of Workflow



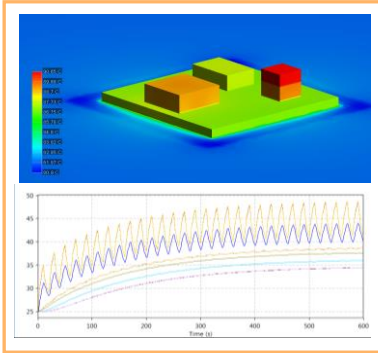
Addressing this flow Bottleneck

- **Enable** RF engineers with ability to perform their own thermal analysis and optimize heat mitigation solutions **during the design phase**
- Requirements
 - **Accessible** - thermal analysis needs to be easy to use, easy to implement (set up), integrated in existing design flows
 - **Fast** – offer significant time savings over alternative (existing) approach
 - **Accurate** – proven thermal solver with high degree of confidence in results and resilient to user errors

Celsius™ Thermal Solver: Electrical-Thermal Co-Simulation

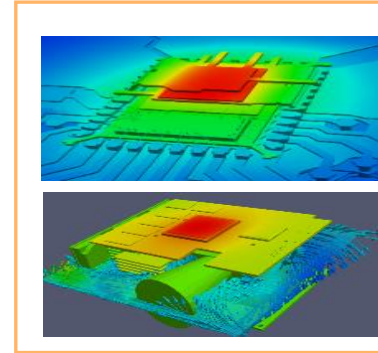
A complete solution for unprecedented performance and accuracy

Chip/PKG/System E-T Co-Simulation



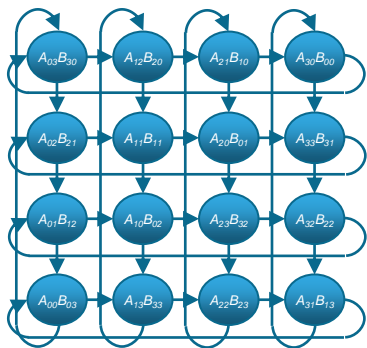
- Includes Chip/3DIC Analysis
- E-T Co-simulation
- Static and Transient

Accuracy Beyond CFD



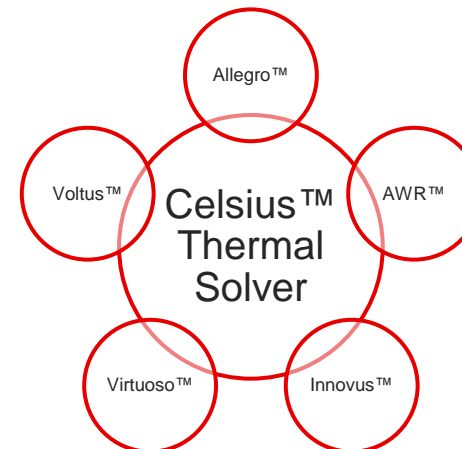
- FEA-CFD integration
- 3D fluid-flow simulation
- Stress Analysis
- Electrical/thermal co-sim

Unprecedented Performance and Capacity



- Massively parallel solver
- Linear scalability, cloud ready
- No loss in accuracy

Integration with Cadence® Design Platforms

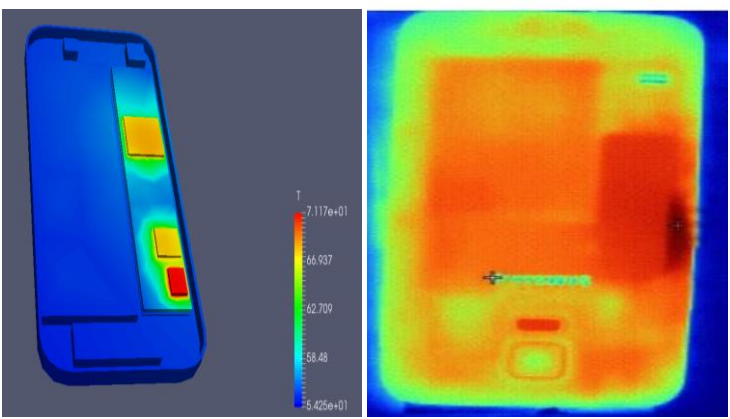


- Single IC, 3D-IC
- Package, PCB
- Chassis, racks, systems

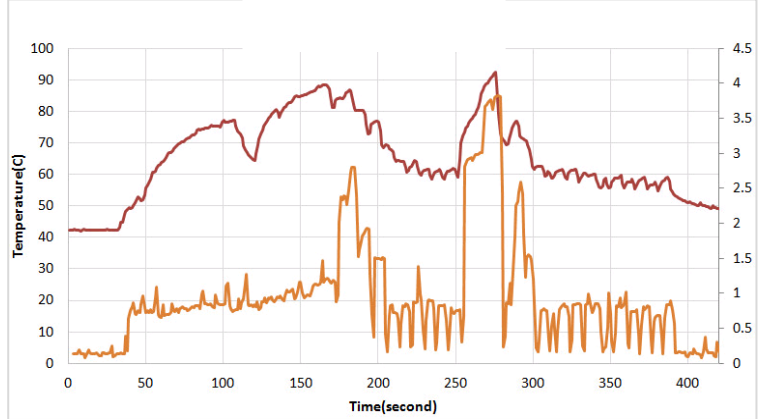
Thermal Profiling in a Mobile Phone

IC-centric electrical-thermal co-simulation - transient analysis and system optimization

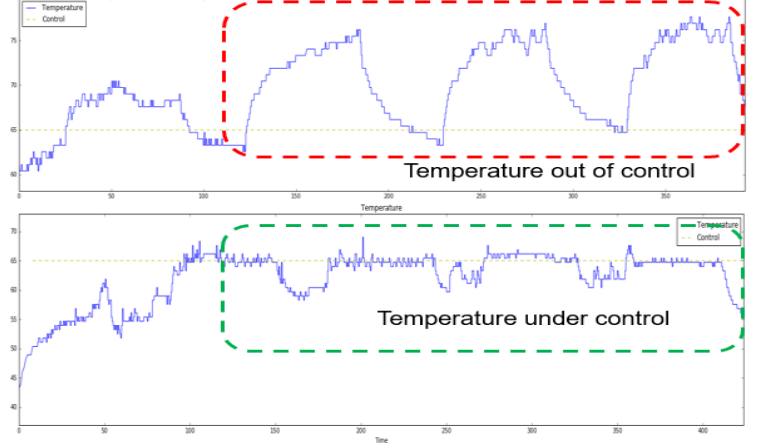
A Complete System: IC/PKG/PCB/Enclosure



CPU Power Profile and Temperature Variations



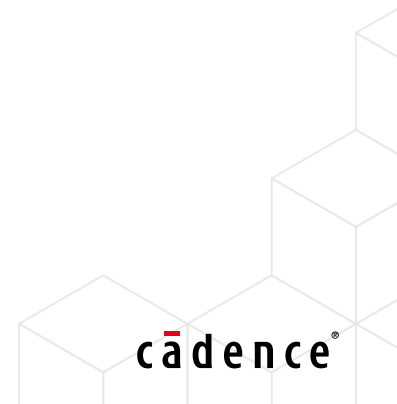
GPU Power Profile and Temperature Variation



Transient thermal • Accurately calculate transient temperatures under various power scenarios

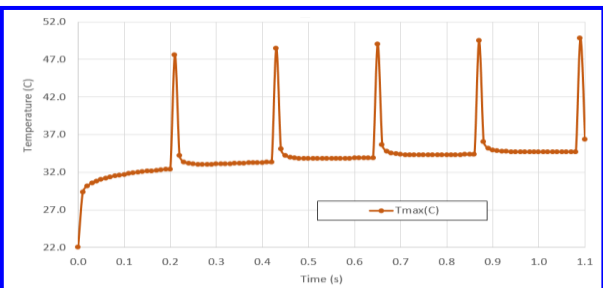
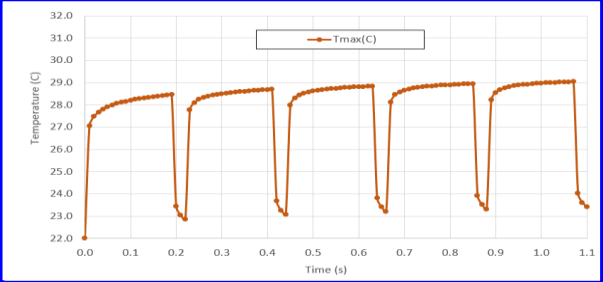
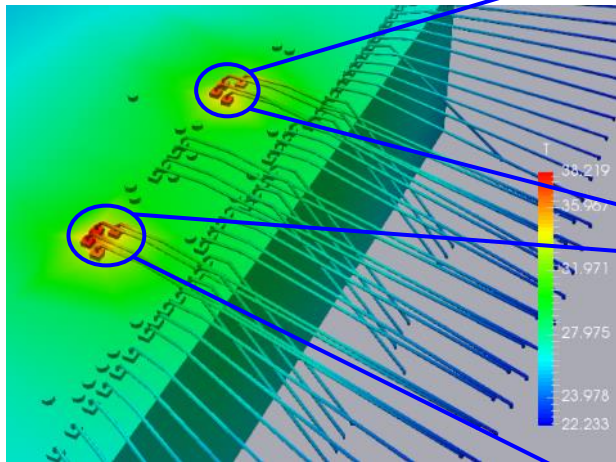
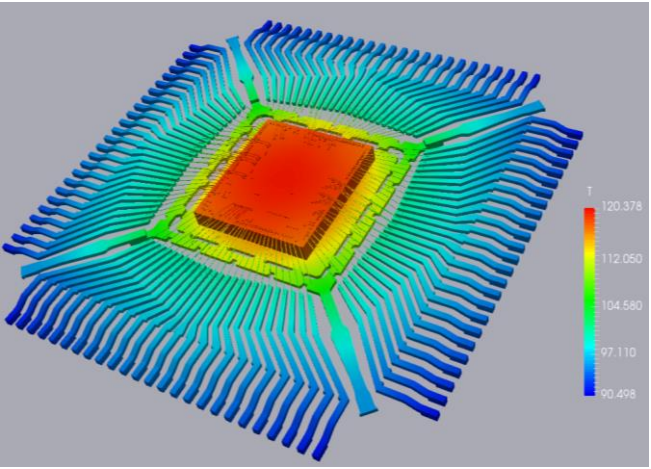
Thermal SPEC verification • Thermal runaway. CPU/GPU DVFS strategy for better thermal performance.

Thermal sensor optimization • Optimization of temperature sensors on chips for detecting thermal runaway
• Find Transient thermal hotspots with detailed power scenarios on each die



Advanced Lead-Frame Package and PCB

Transient Electrical-Thermal Analysis with Resolution of 3D Configuration



Design Import

- Package design imported from SiP layout
- 3D structures created from SiP design

Electrical-Thermal Co-sim

- Detailed power profiling from chip simulation
- Additional power source from electric current
- Pulsed current going through bond wires

Thermal Results

- Transient and static analysis results generated
- Detailed temperature profiles on bond wires

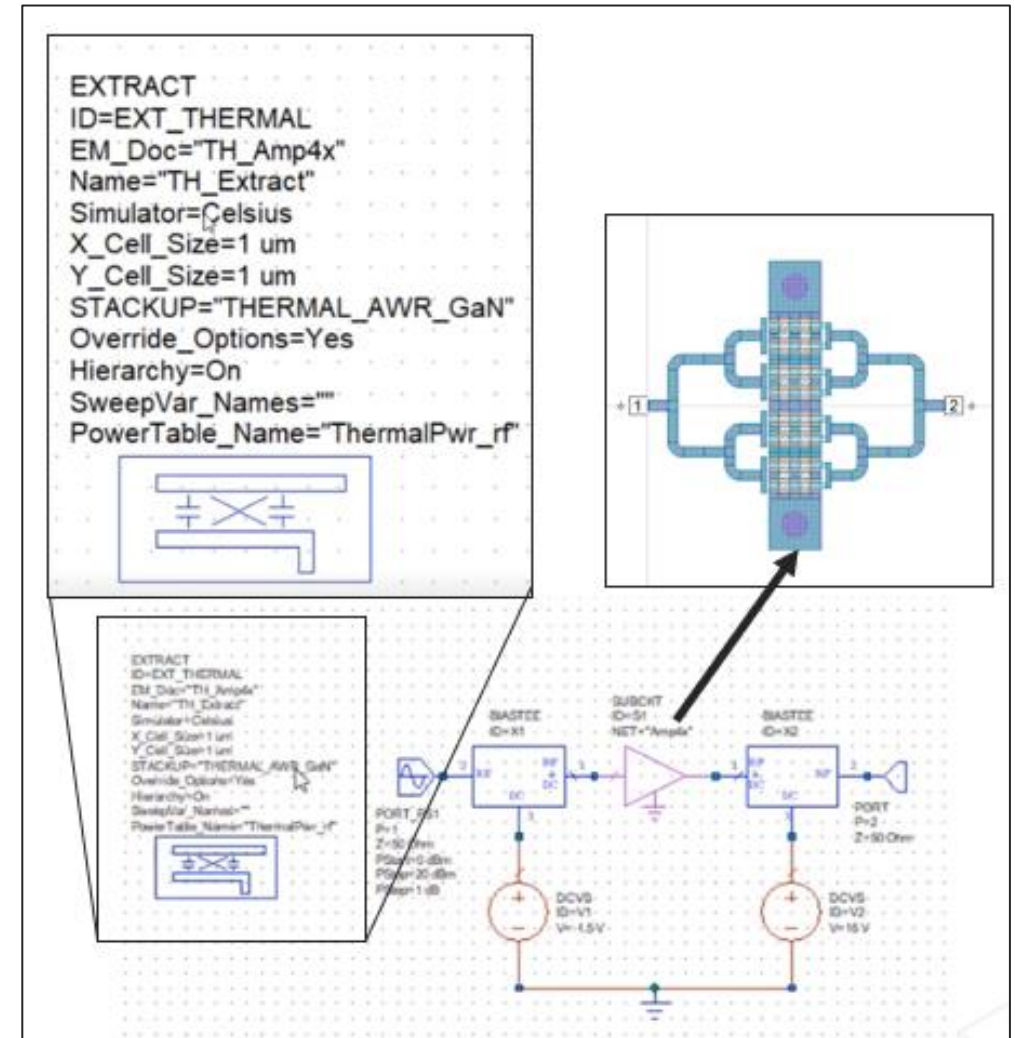




In-Design Enablement

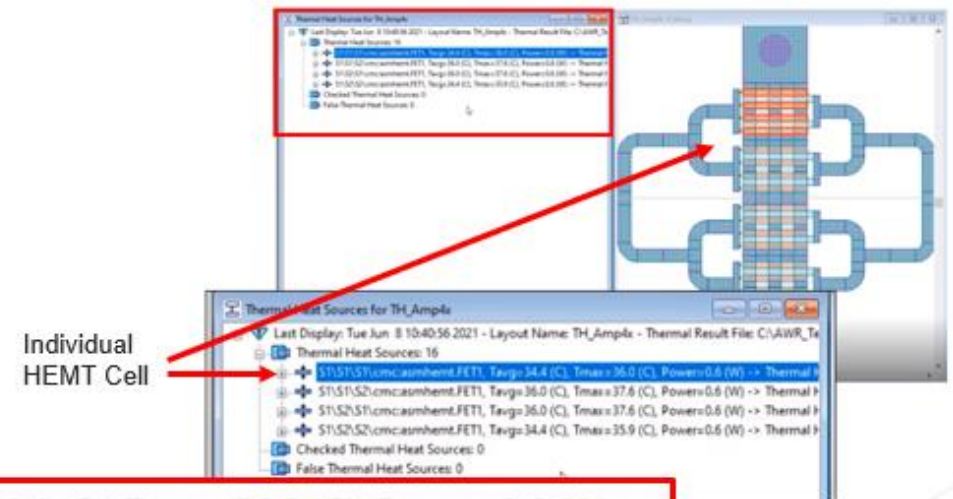
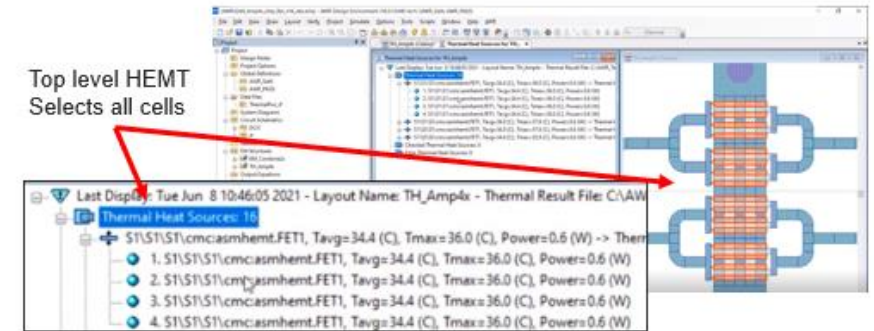
Thermal Extraction Setup – GaN FET Example

- **Add extraction block** to create thermal document
- New measurement - creates **power dissipation** data file from nonlinear simulation
- Associate extraction block with stackup and power dissipation data file
- Simulate in Microwave Office[®] software or send to Celsius[™] Thermal Solver (native editor)
- Operating temps back-annotated into Microwave Office[®] and linked to user defined heat sources



Thermal Analysis Results – GaN FET Example

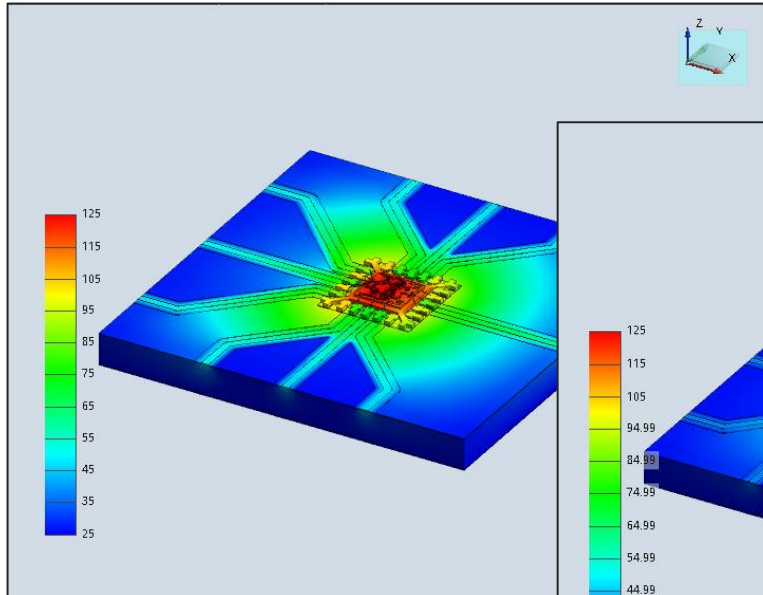
- Test structure – GaN HEMT devices, combiner network and source to ground vias
- Celsius™ Thermal Solver results automatically provides list of all defined heat sources throughout hierarchal design layout
- Selected thermal analysis results for individual heat source are highlighted in layout
- Average and peak temperature across heat source area and power dissipation are reported



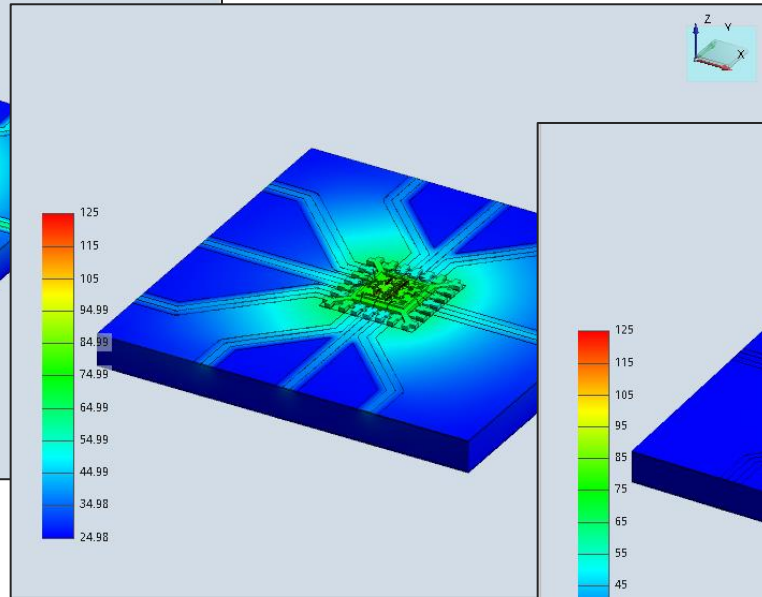
1. S1\S1\S1\cm:asmhemt.FET1, Tavg=34.4 (C), Tmax=36.0 (C), Power=0.6 (W)

Thermal Analysis Results – Multi Technology Example

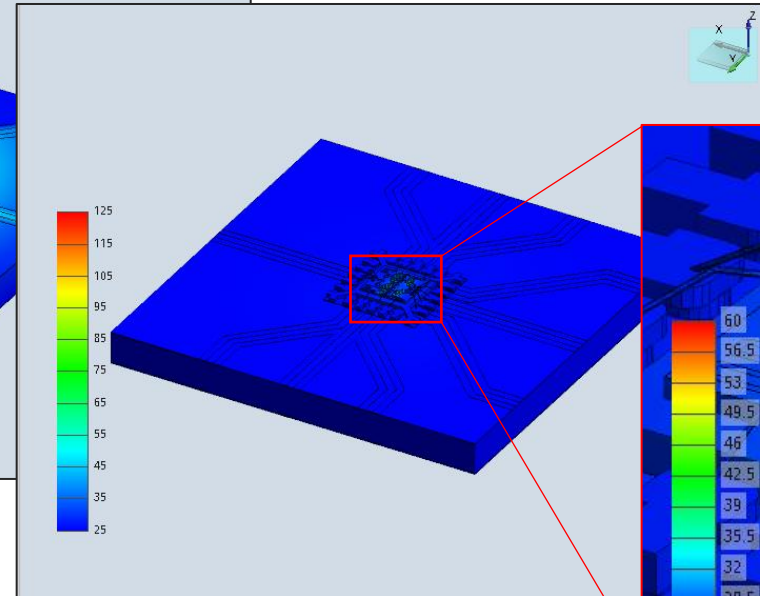
- Test structure – MMIC HPA in QFN package on PCB (identical temperature scale to 125 °C)



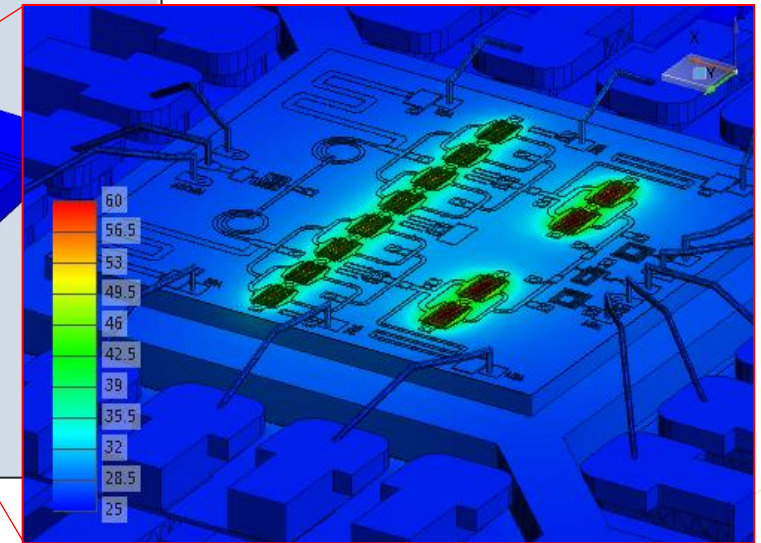
No thermal relief



Thermal vias under QFN

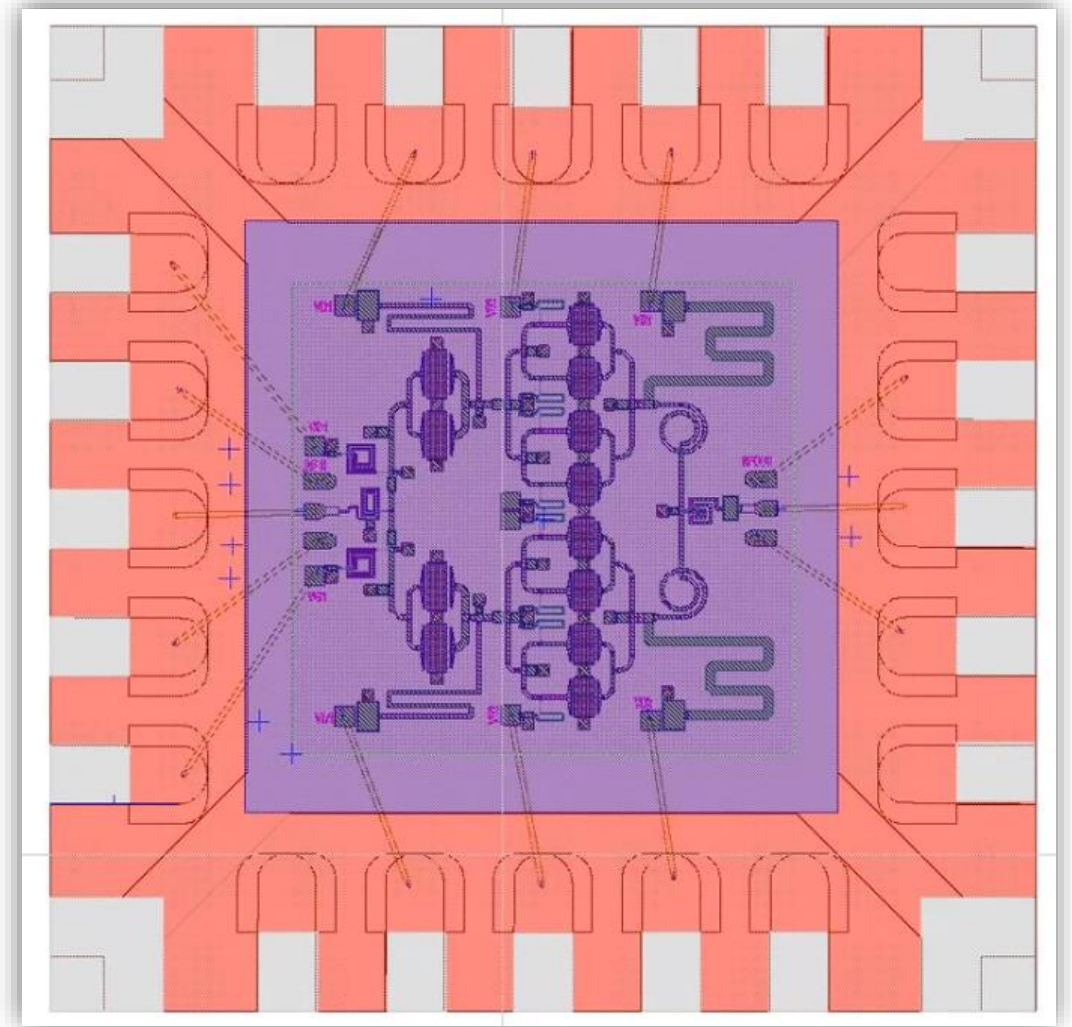
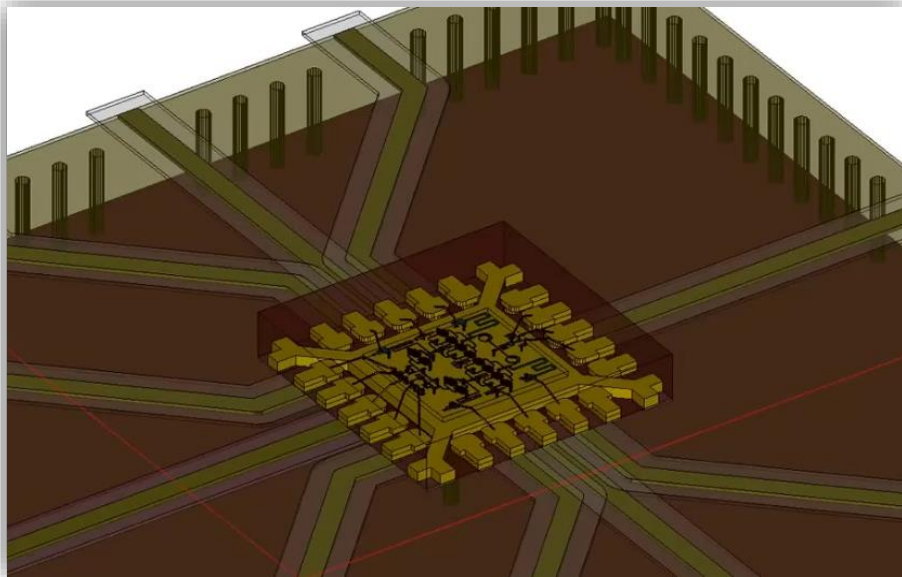
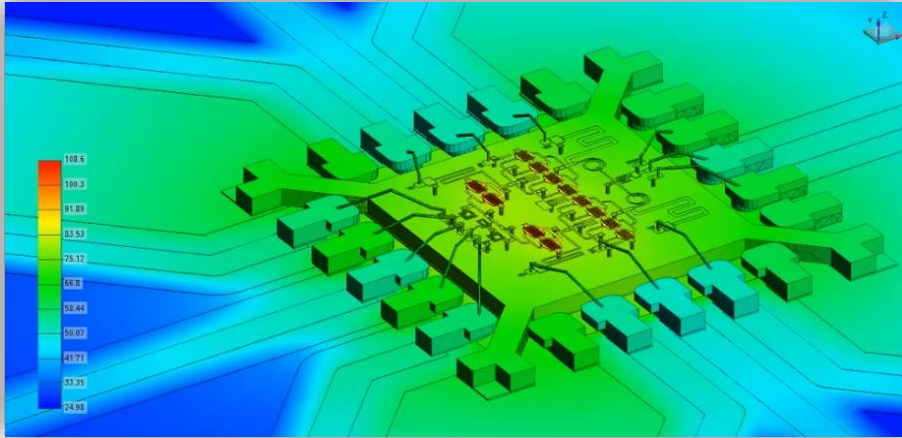


Heatsink under QFN



Enlarged view (60 °C temperature scale)

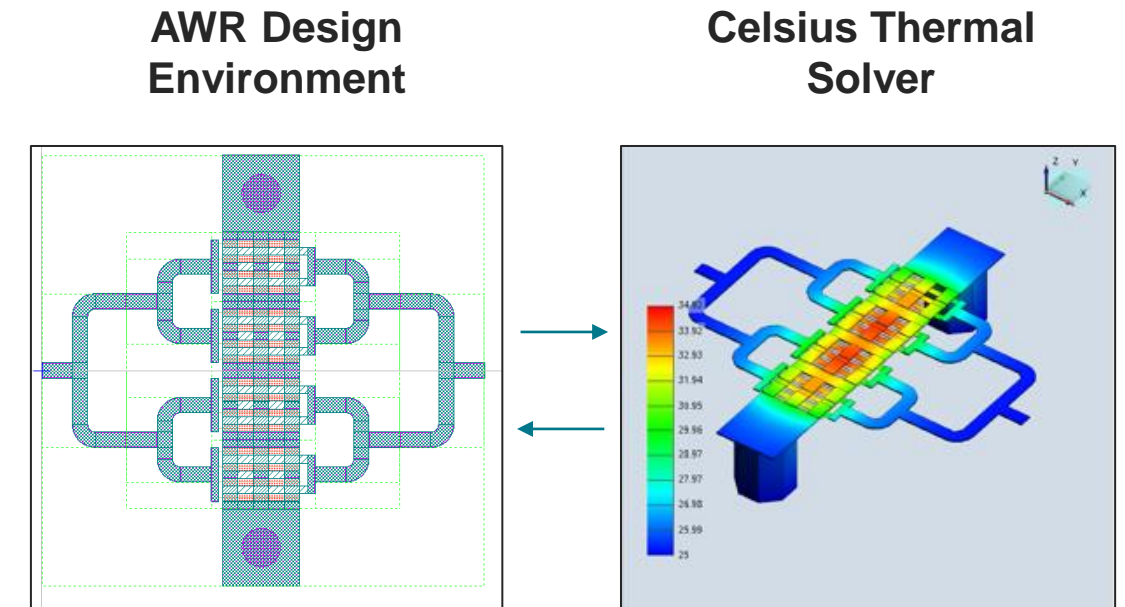
Please Contact us for a Demo!



Celsius Thermal Solver for Thermal Analysis in Microwave Office Software

Key features and benefits

- Thermal structures are easily created using powerful Microwave Office[®] extraction block workflow
- Leverages existing structure data (geometries, materials, stack up) in Microwave Office software to define Celsius[™] structure
- Obtain power dissipation information from Microwave Office analysis
- Thermal simulations launched from inside AWR platform; results automatically returned
- Easy-to-use flow allows RF design engineers to perform their own thermal analysis





Summary

Cadence RF Electrothermal = Speed, Accessibility, Accuracy

- Predicting thermal behavior of RF designs is very important to ensure reliability and performance
- Traditional flows for thermal characterization are too slow and error prone to provide design-side guidance
- AWR/Celsius integration
 - Saves design re-entry
 - Utilizes existing data structure in AWR as enable
 - Provides near real-time access to critical thermal data using a sign-off quality thermal environment



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