

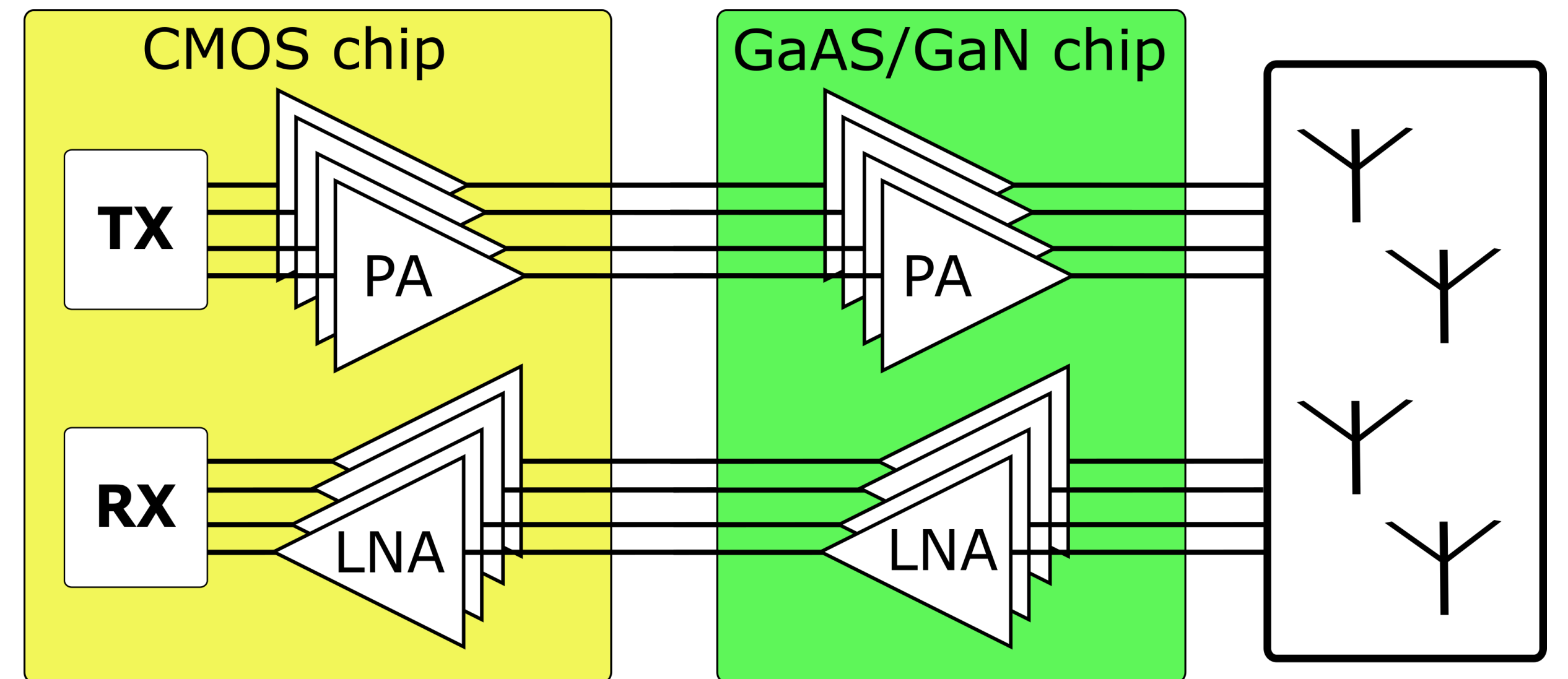
IC research directions GaN / GaAs – CMOS co-design

Kaisa Rynnänen, Kari Stadius, Jussi Rynnänen
AALTO UNIVERSITY

- ❖ Veturi program
- ❖ Business Finland

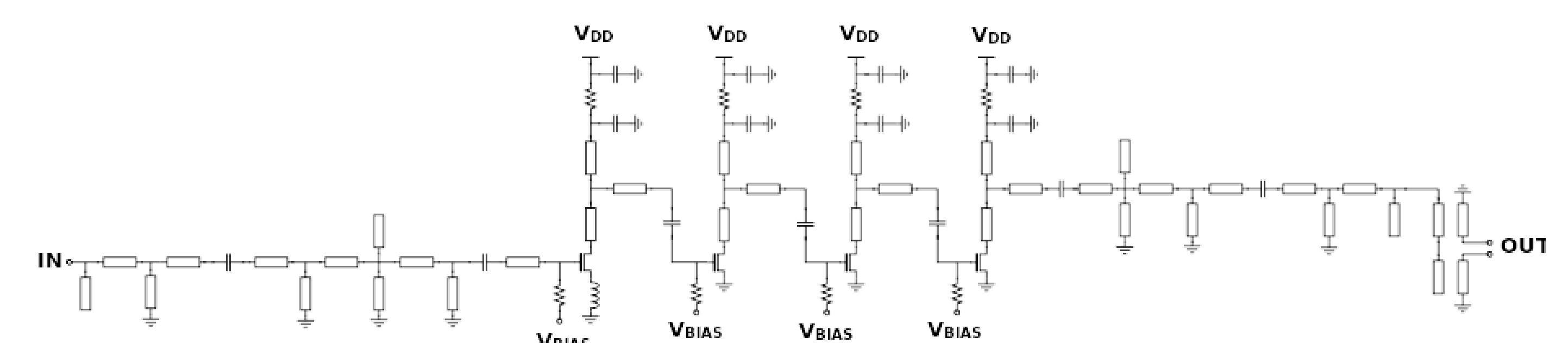
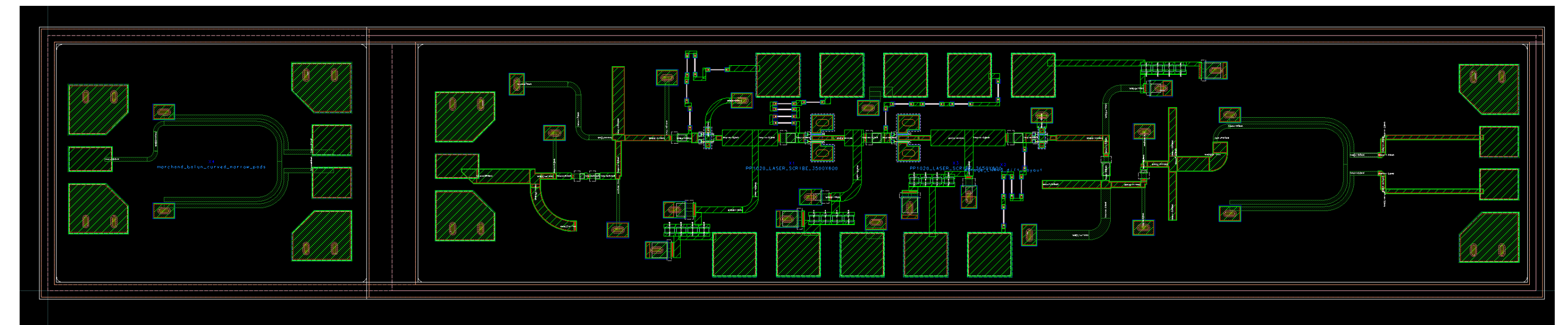
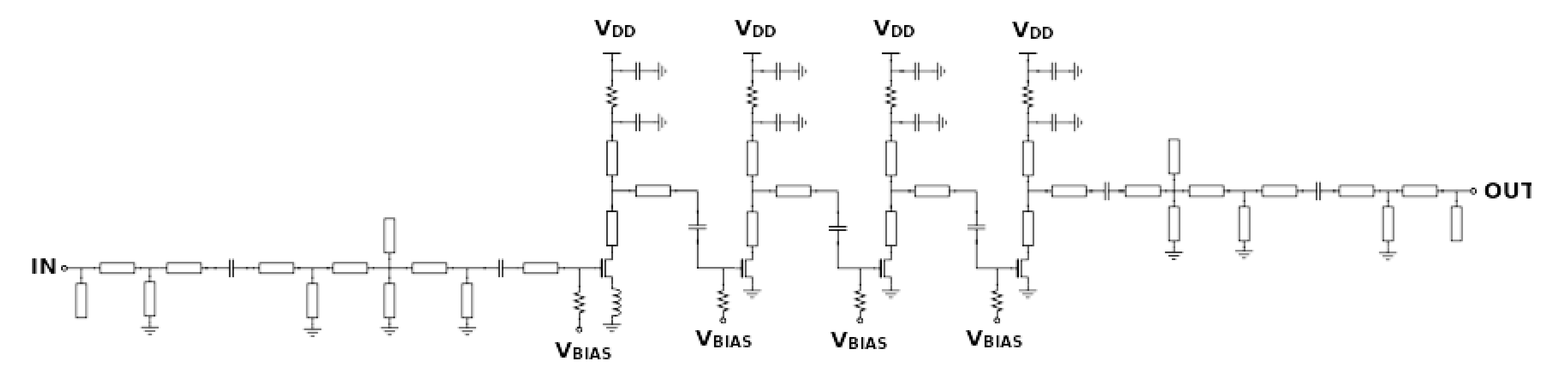
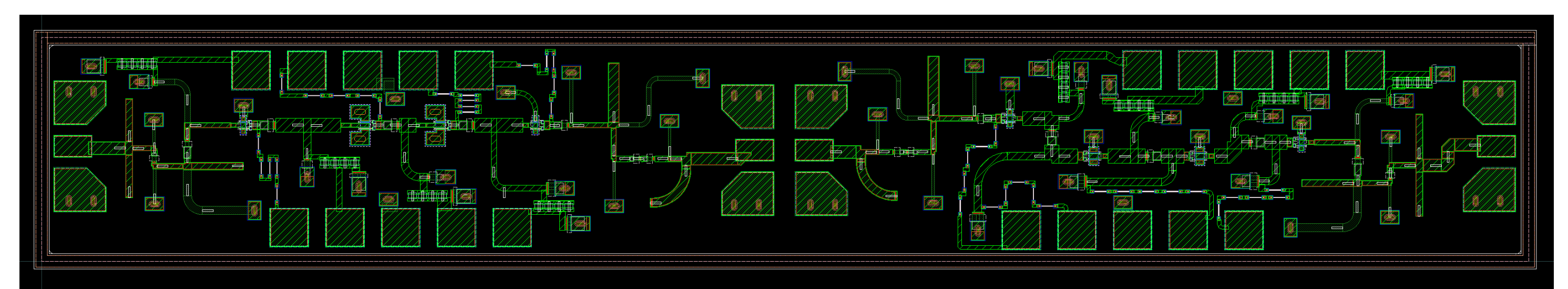
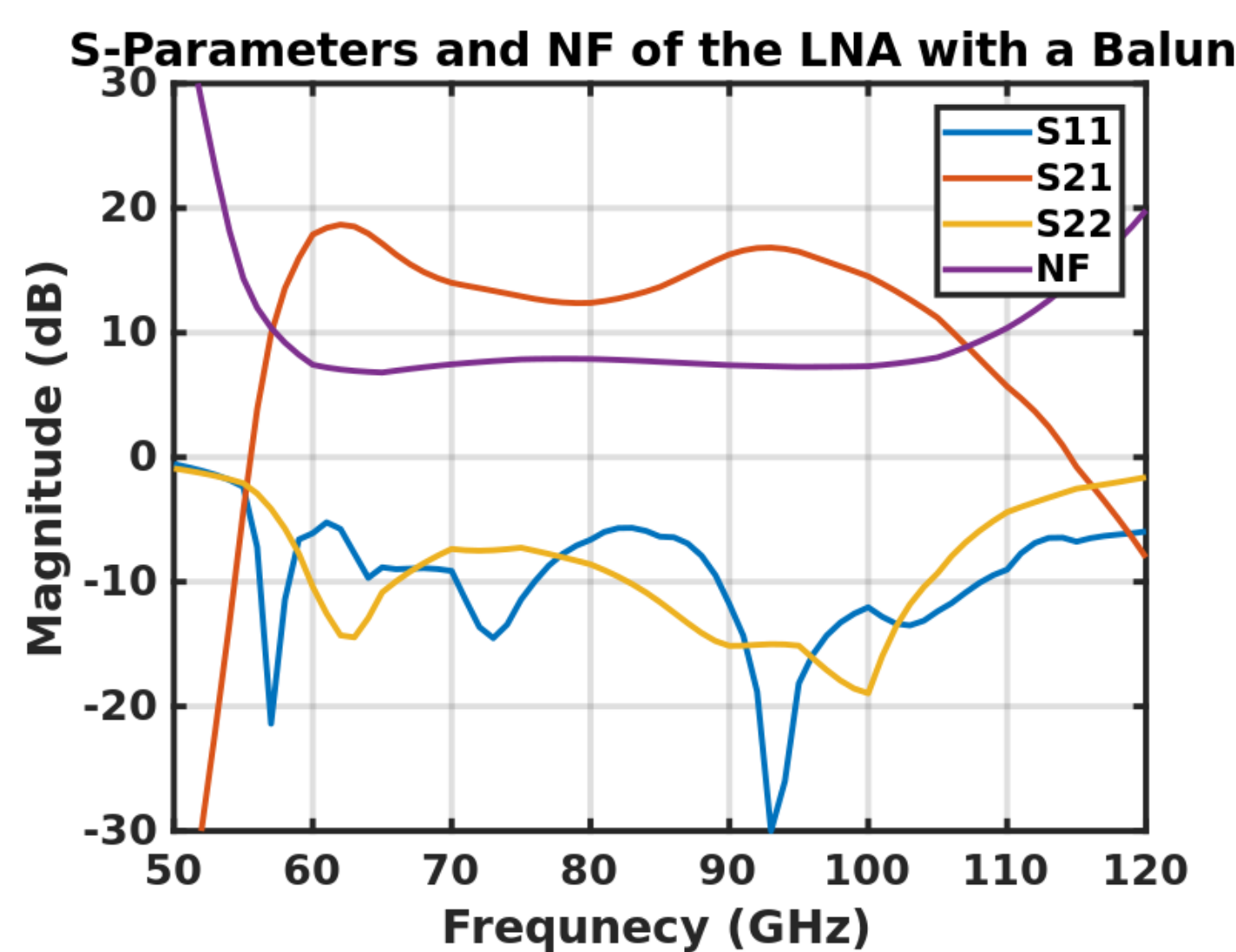
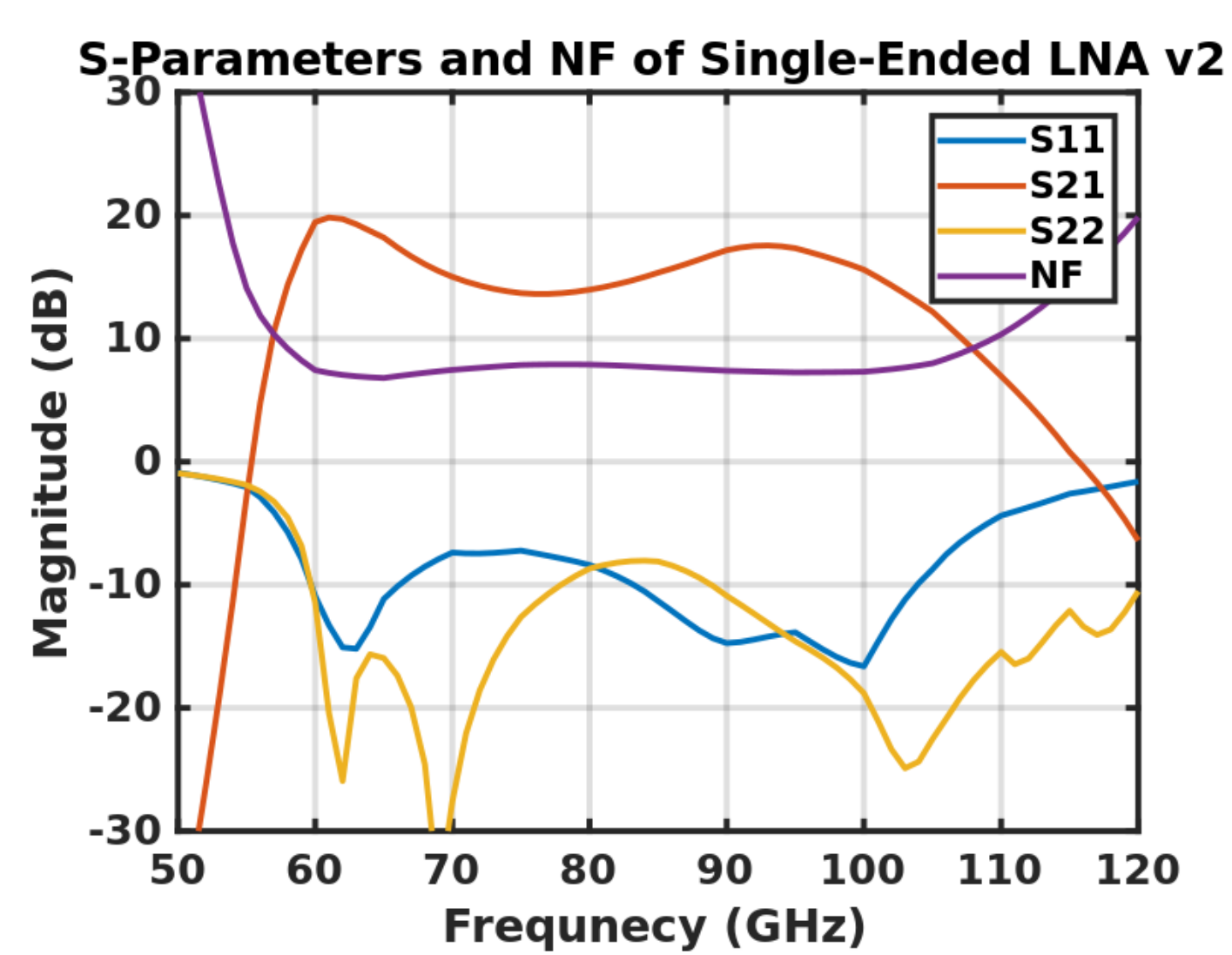
Motivation

- ❖ GaN /GaAs front-ends offer higher sensitivity and better power efficiency
- ❖ GaN booster die enables high output power
- ❖ 3D-integration enables dense phased array implementations



GaAs LNA

- ❖ Wideband four-stage pre-amplifier for a CMOS receiver with a 0.1 μm GaAs pHEMT technology
- ❖ Three versions have been designed with single-ended and balanced output
- ❖ BW=60...100 GHz, Gain=15 dB, NF=8 dB, DC = 27 mA / 1V
- ❖ Die size 4 x 0,6 mm



GaN PA, LNA and VCO

- ❖ Aalto's first tape-out on 0.15 μm GaN D-HEMT process
- ❖ A learning experience: simple LNA, PA, VCO
- ❖ Sensors for temperature analysis

LNA is a current re-use two-stage amplifier:

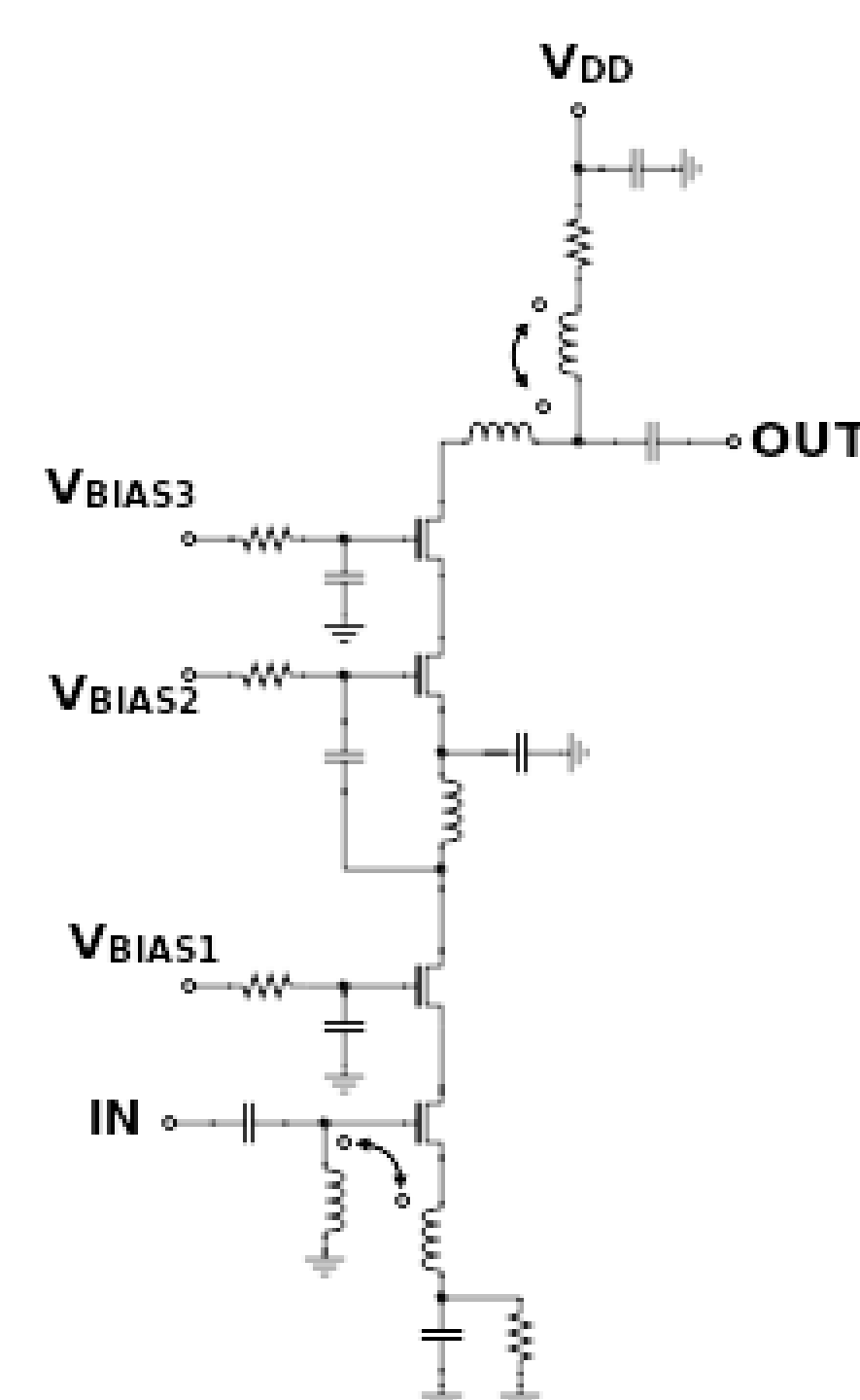
At 25 GHz Gain =14 dB, NF=3 dB, Pin,1dB=-13dBm

PA is a three-stage amplifier operating at 25 GHz:

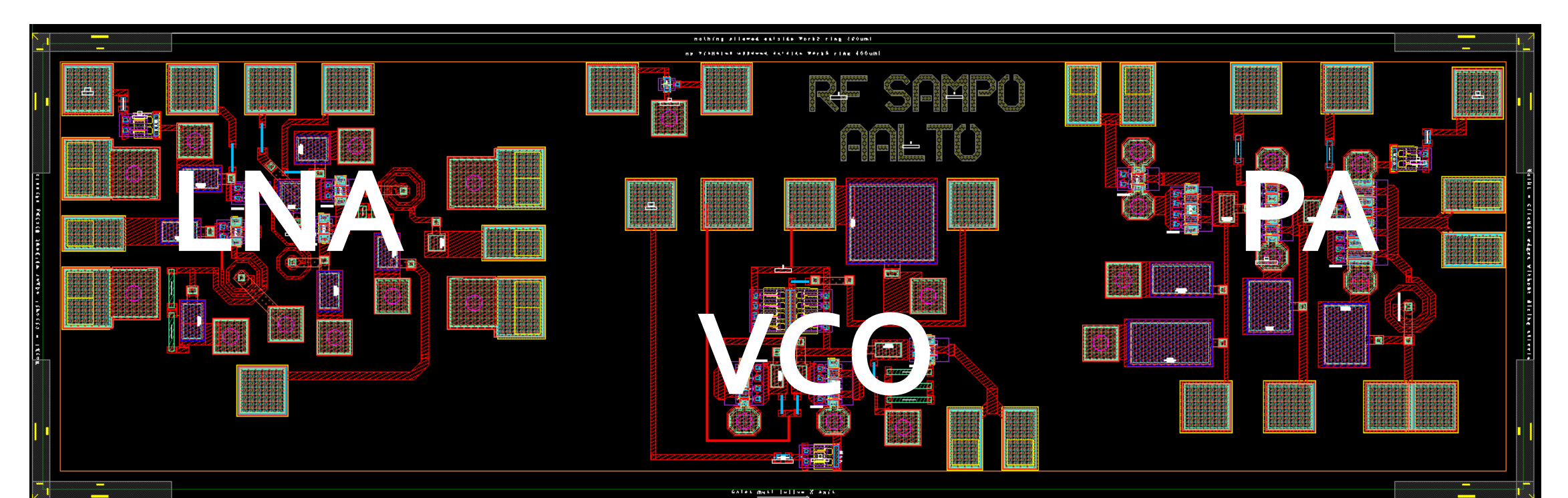
Gain=23 dB, Pout,1dB=26 dBm, DC= 260 mA / 10V

VCO is a cross-coupled transistor-pair LC-oscillator:

Freq=25-29 GHz, phase noise = -116 dBc/Hz@1MHz at 29 GHz



Current re-use LNA



Die size 3 x 1 mm

Acknowledgement

GaAs LNA work has been conducted in co-operation with a research group of professors G. Lasser and C. Fager from Chalmers University, Sweden.