Model-Based RF Development in Complex Radio Systems – case: Power Amplifier Digital Pre-distortion

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Outline

- Background and Motivation
- Trend for digital transformation in engineering
- Iterative model-based radio design flow high level view
- Use-Case: PA linearization with DPD technique
 - Accurate PA behavioural modelling
 - PA-DPD sub-system design & verification flow
- Importance of simulation confidence and how to build it
- Comparison of virtual PA-DPD simulation results with measurements



Background – ever increasing complexity Moving towards 6G communications

Complexity of massive MIMO radio systems is getting higher

- SW code lines per radio > hundreds of millions...
- HW component count per radio > 30k...
- More signal processing at the radio
- Higher operating frequencies up to sub-THz range
- 2.5/3D SoC chiplet designs & higher power densities
- Product requirements > 1k....
- Customer use-cases > 1k...
- ML/AI embedded inside a radio



Al's Illustrated Vision of Next Gen Wireless Cell Tower

Solution – Digital Engineering Model-based & automated AI guided design processes



Engineering transformation to digital era

Digital Twins Digital Thread Agile HW & SW development AI powered data analytics Cloud Computing Industrial Metaverse



MBD case: Power Amplifier (PA) linearization with DPD technique Why Digital Pre-Distortion (DPD) is needed ?

The DPD signal processing algorithm compensates for an amplifier's nonlinearities, letting it operate in its nonlinear region for maximum power efficiency.



Power Amplifier (PA) modelling

Raising the model abstraction level for speeding up the system simulations

- The models of PA transistors or integrated modules are typically provided as compact circuit models from the device vendors
- The compact circuit models are computationally very slow for sampled communication systems
- It is possible to generate a fast behavioral model from a circuitbased PA simulations or measurements, and still provide sufficient accuracy including following important RF impairment effects:
 - ➢ Non-linearities
 - Short & long-term memory effects
 - ➤ Load-pull effects (optional)
- The PA-DPD sub-system simulation time can be reduced from tens of hours to minutes with the use of a behavioral model.

Trade-off between models



PA-DPD sub-system design & verification flow MBSE driving for AIL/MIL/SIL/EIL/FIL verification tests



DESIGN FLOW - INCREASING FIDELITY AND CONFIDENCE LEVEL BEFORE SOC TAPE-OUT

VUVIJ

SHIFT-LEFT VERIFICATION ACTIVITIES

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*) A Virtual TLM prototype can fully mimic the functionality of a target System-on-Chip (SoC) and run embedded SW code on it.

PA-DPD Functional Architecture Verification Algorithms-in-the-loop (AIL) test with a virtual PA model



Functional DPD architecture Model

- The functional system model of the PA-DPD is verified using the AIL simulation process shown on the right.
- After simulation the system requirements can be validated.



Typical simulation outputs: SNR, Pave, PAR, ACLR, EVM, AM/AM, AM/PM

Virtual executable PA-DPD test setup in Simulink

PA-DPD Functional Architecture Verification Algorithm-in-the-loop (AIL) test with a real physical PA



Functional DPD architecture Model

- The functional system model of the PA-DPD is verified using the hybrid AIL process shown on the right.
- After simulation the system requirements can be validated.



Hybrid PA-DPD test setup



Simulation confidence

Digital engineering success is linked with confidence





Improving simulation confidence at all design abstraction levels is one of the key goals in digital engineering transformation.

High-confidence on early results will maximize business value in terms of TTM*, Cost, Quality.

Building the simulation confidence

Continuous comparison of virtual prototypes against real prototypes



Practical PA-DPD system analysis example with AIL tests Comparison of simulations and measurements at instantaneous signal BW of 200 MHz

Normalized dynamic gain of a PA, showing its memory and non-linearity effects w/o DPD



Modulated input signal = $2 \times 100 \text{ MHz} 5\text{G-NR}$





Modulated input signal = $2 \times 100 \text{ MHz} 5\text{G-NR}$

